

REVISIONS			
LTR	DESCRIPTION	DATE	APPR
A	ECO_570	11/8/05	
B	ECO_736 (S3R was S3)	10/10/06	

SPECIFICATION ADDENDUM, 24 Bit Serial Synchronous Interface SSI:

SSI output provides effective synchronization in a closed-loop control system. A clock pulse train from a controller is used to shift out sensor data: one bit of position data is transmitted to the controller per clock pulse received by the sensor. The use of a differential driver permits reliable transmission of data over long distances in environments that may be electrically noisy. The encoder utilizes a clock signal, provided by the user interface, to time the data transmission. Receiving electronics must include an appropriate receiver as well as line terminating resistors. A parity bit is standard to validate the transmitted data. Non-volatile zero reset (optional) is available.

Features:

- Synchronous transmission
- RS422/485 compatible
- Transmission lengths to 1000 feet
- Clock rates from 70 KHz to 1.8 MHz
- Parity bit is standard
- Non-volatile zero reset (optional)

Data Transmission Sequence:

1. Data from the encoder is sent with a MAX 491ESD transceiver in transmit mode. It is recommended to use any RS-422/485 compatible receiver and provide a termination resistor based on the RS-422/485 specification for your specific voltage and DATA line length.
2. The CLOCK signals are RS-422/485 compatible, differential TTL, with 180 Ohm termination resistors internal to the encoder. Reference: CLOCK line timing diagram to advance data.
3. On the first HIGH-to-LOW CLOCK transition, the encoder latches its data at the current position and prepares to transmit. The DATA signal during this transition is a START bit, which is always HIGH.
4. The encoder shifts data to the DATA line on each LOW-to-HIGH clock transition, beginning with T11 (the MSB). The controller reads data on the HIGH-to-LOW transition of the next 25 clock cycles where the 24th clock cycle is F0 (the LSB). The parity bit is clocked out on the 25th clock cycle. When the parity option is not used, the 25th bit output is a logic LOW.
5. Parity is even. The sum of all data bits and the parity bit is even.
6. After the last CLOCK LOW-to-HIGH transition, a minimum of 30 microseconds must pass before the beginning of the next CLOCK series.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES APPLY AFTER FINISH TOLERANCES ON .XX ±.01 .XXX ±.005 ANGLES ± 0° 30' REMOVE BURRS AND BREAK ALL SHARP EDGES .010 MAX ALL DIA. TO BE © WITHIN .010	redrawn KRB <i>[Signature]</i> DATE 11/8/05	BEI INDUSTRIAL ENCODER DIVISION BEI TECHNOLOGIES, INC. 7230 Hollister Avenue Goleta, CA 93117-2891 Tel: (805) 968-0782 Fax: (805) 968-3154			
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	ENGR		TITLE SPECIFICATION ADDENDUM 24 Bit Serial Synchronous Interface (SSI)		
	APPR <i>LS</i>	4-24-08			
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		SCALE: NONE	924-02087-002b	SHEET: 1/3	

Interfacing Long Data Lines:

Cable impedance creates a transmission delay, shifting the phase relationship between the clock pulse and the data. If this pulse shift exceeds 180°, then the wrong bit position will be sampled by the receiver. The maximum allowable clock frequency, therefore, is a function of the cable length. For 24 AWG, stranded, 3 pair cable (BEI part number 37048-003 or equivalent) the group delay is 1.36nS/ft. The table below shows the maximum transmission rate allowable as a function of cable length to ensure a phase shift of less than 90°.

CLOCK: Maximum (KHz) = 92,000/Cable Length (ft)

Cable Length (feet)	50	100	200	300	500	1000
Max. Frequency (KHz)	1800	900	500	300	200	100

SSI Compatible Serial Code (S3):

FUNCTION	CONNECTOR*	CABLE	TERM BOARD	
			H40	H38
DATA+	A	YEL	1	4
DATA-	H	WHT/YEL	7	7
CLOCK+	B	BLU	2	5
CLOCK-	I	WHT/BLU	8	8
DIRECTION CONTROL	C	ORN	3	6
ENABLE (OPTIONAL)	E	VIO	-	9
RESET (OPTIONAL)	J	WHT/ORN	9	10
SUPPLY VOLTAGE (+V)	D	RED	4	3
CIRCUIT COMMON (0V)	F	BLK	5	2
CASE GROUND	G	GRN	6	1

*Connector is a MS3102E18-1P, 10-pin connector on the encoder body and mates to an MS3106F18-1S connector or can be used with a standard cable/connector assembly, BEI P/N: 924-31186-18XX.
(XX = cable length in feet, ie. 10 = 10 feet)

Direction Control: Direction Control is standard on the HMT25 series. If this function is not used, then the encoder will show a CW increasing count when viewed from the shaft end. Direction Control (Pin C) is normally HIGH and is pulled up internally to the positive supply voltage. To reverse the count direction, Pin C must be pulled LOW (signal common).

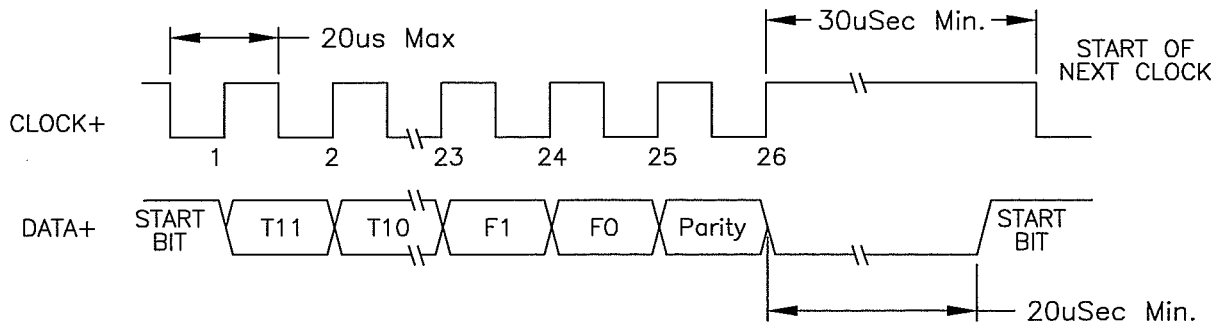
Reset (option): The reset pin (Pin J) is normally HIGH and is pulled up internally to the positive supply voltage. To activate the Reset function, Pin 'J' must be pulled LOW by connecting it to signal common for 1 Sec or greater while the encoder shaft is stationary. This causes the present encoder position to be stored into non-volatile memory as an offset value and the output of the encoder is then set to the value of '0'. The encoder will retain this offset even if the power is turned off and on again. A new '0' position can be set by rotating the encoder shaft to a new position and then activating the Reset pin again.

Enable (option): This option allows the operator to momentarily deactivate the outputs from the encoder. This may be useful in instances where the outputs from several different encoders must be sampled independently. This pin is normally HIGH (Enabled) and is pulled up internally to the positive supply voltage. To deactivate the Enable function Pin 'E' must be pulled LOW (signal common). The outputs then become high impedance (Tri-State).

BEI INDUSTRIAL ENCODER DIVISION
BEI TECHNOLOGIES, INC.

SIZE A	FSCM NO. 1RB90	DWG NO. 924-02087-002	REV B
SCALE: NONE		SHEET: 2/3	

24 Bit, SSI Compatible Output with Parity Timing Diagram:



T11 = MSB, Turns Count

F0 = LSB, Fine Count

Note: Unused bits are transmitted as logical zeros

Example Model Number:

Encoder: HMT25D - F1 - SS - 12X12NB - S3R - CW - SM18 - S

SSI	S3
SSI	S3R
WITH RESET	

Specials:
Output Enable