

REVISIONS			
LTR	DESCRIPTION	DATE	APPR

SPECIFICATION ADDENDUM, Serial Synchronous Interface 14-15 bit (SSI):

SSI output provides effective synchronization in a closed-loop control system. A clock pulse train from a controller is used to shift out sensor data: one bit of position data is transmitted to the controller per clock pulse received by the sensor. The use of a differential driver permits reliable transmission of data over long distances in environments that may be electrically noisy. The encoder utilizes a clock signal, provided by the user interface, to time the data transmission. Receiving electronics must include an appropriate receiver as well as line terminating resistors. An optional parity bit is available to validate the transmitted data.

Features:

- Synchronous transmission
- RS422/485 compatible
- Transmission lengths to 1000 feet
- Accepts clock rates from 100 KHz to 1.8 MHz
- Parity bit option is available

Data Transmission Sequence:

1. Data from the encoder is sent with a MAX 491 transceiver in transmit mode. It is recommended to use any RS-422/485 compatible receiver and provide a termination resistor based on the RS-422/485 specification for your specific voltage and DATA line length.
2. The CLOCK signals are RS-422/485 compatible, differential TTL, with 180 Ohm termination resistors internal to the encoder. A series of pulses from the controller, on the CLOCK lines, advances the data.
3. On the first HIGH-to-LOW CLOCK transition, the encoder latches its data at the current position and prepares to transmit. The DATA signal during this transition is a START bit, which is always HIGH.
4. The encoder shifts data to the data line on each LOW-to-HIGH CLOCK transition, beginning with the MSB. The controller reads data on the HIGH-to-LOW transition of the next 16 CLOCK CYCLES ending with parity (optional and = logic 'lo' if not specified). Bit 15, if specified, is provided on the 15th CLOCK CYCLE and = logic 'lo' if 14 Bit encoder is specified.
5. Parity is even. The sum of all data bits and the parity bit is even.
6. After the last CLOCK HIGH-to-LOW transition, a minimum of 40 microseconds must pass before the beginning of the next CLOCK series.

UNLESS OTHERWISE SPECIFIED
 DIMENSIONS ARE IN INCHES
 APPLY AFTER FINISH
 TOLERANCES ON
 .XX ±.01
 .XXX ±.005
 ANGLES ± 0° 30'
 REMOVE BURRS AND BREAK ALL
 SHARP EDGES .010 MAX
 ALL DIA. TO BE © WITHIN .010

redrawn	KRB	DATE	5/15/07
CHECKED	N/A		
ENGR	N/A		
APPR	LC		7-24-08

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TITLE
 SPECIFICATION ADDENDUM
 SERIAL SYNCHRONOUS INTERFACE
 14-15 BIT (SSI)

SIZE	FSCM NO.	DWG NO.	REV
A	1RB90	924-02087-003	-

SCALE: NONE	924-02087-003	SHEET: 1/2
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Interfacing Long Data Lines:

Cable impedance creates a transmission delay, shifting the phase relationship between the clock pulse and the data. If this phase shift exceeds 180°, then the wrong bit position will be sampled by the receiver. The maximum allowable clock frequency, therefore, is a function of the cable length. For 24 AWG, stranded, 3 pair cable (BEI part number 37048-003 or equivalent) the group delay is 1.36nS/ft. The table below shows the maximum transmission rate allowable as a function of cable length to ensure a phase shift of less than 90°.

CLOCK: Maximum (KHz) = 92,000/Cable Length (ft)

Cable Length (feet)	50	100	200	300	500	1000
Max. Frequency (KHz)	1800	900	500	300	200	100

SSI Compatible Serial Code (S3):

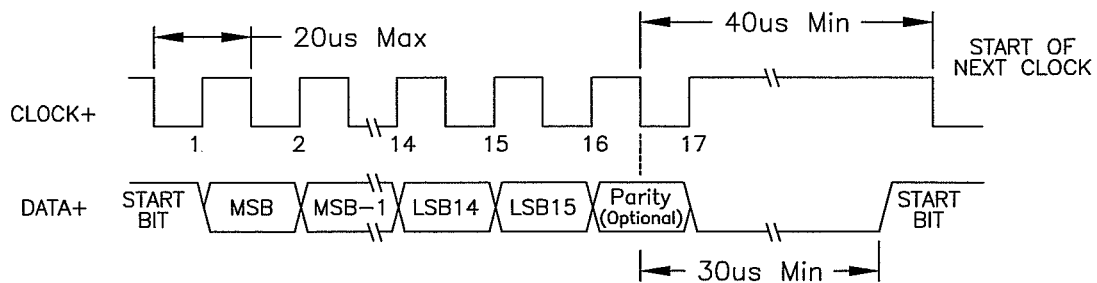
FUNCTION	CABLE	CONNECTOR		TERM BOARD	
		M18*	M14/19**	H40	H38
DATA+	YEL	A	A	1	4
DATA-	WHT/YEL	H	B	7	7
CLOCK+	BLU	B	C	2	5
CLOCK-	WHT/BLU	I	D	8	8
DIRECTION CONTROL	ORN	C	R	3	6
ENABLE (OPTIONAL)	WHT/ORN	J	P	9	9
SUPPLY VOLTAGE (+V)	RED	D	V	4	3
CIRCUIT COMMON (0V)	BLK	F	T	5	2
CASE GROUND	GRN	G	S	6	1
SHIELD DRAIN	BARE	-	-	-	-

*Connector is a MS3102R18-1P, 10-pin connector on the encoder body and mates to an MS3106F18-1S connector or equiv. Can be used with a standard cable connector assembly, BEI P/N: 924-31186-18XX (XX = cable length in feet, i.e., 10, 20, 30 = 10, 20 or 30 feet respectively)

**Connector is a MS3112E14-19P, 19 pin connector on the encoder body and mates to an MS3116F14-19S connector or equiv. For new part numbers, use M18 connector

Direction Control: Standard is CW for increasing count when viewed from the shaft end. Direction Control Pin is normally HIGH (or N/C) and is pulled up internally to the positive supply voltage. To reverse the count direction, this pin must be pulled to LO (0V)

SSI Compatible Output with Parity Option Timing Diagram:



Example Encoder Model Number:

H25X - SS - 14NB - S3 - CW - SM18 - S

To specify
SSI Output

Specials:
-S = Parity Bit

BEI INDUSTRIAL ENCODER DIVISION
BEI TECHNOLOGIES, INC.

SIZE A	FSCM NO. 1RB90	DWG NO. 924-02087-003	REV -
SCALE: NONE		SHEET: 2/2	