

REVISIONS			
LTR	DESCRIPTION	DATE	APPR
-	ECO_947 (RELEASE)	11/8/07	
A	ECO_1074 Update Add 13 bit W/O parity diag	7/14/08	

### SPECIFICATION ADDENDUM, Serial Synchronous Interface 13 bit (SSI):

SSI output provides effective synchronization in a closed-loop control system. A clock pulse train from a controller is used to shift out sensor data: one bit of position data is transmitted to the controller per clock pulse received by the sensor. The use of a differential driver permits reliable transmission of data over long distances in environments that may be electrically noisy. The encoder utilizes a clock signal, provided by the user interface, to time the data transmission. Receiving electronics must include an appropriate receiver as well as line terminating resistors. An optional parity bit is available to validate the transmitted data.

#### Features:

- Synchronous transmission
- RS422/485 compatible
- Transmission lengths to 1000 feet
- Accepts clock rates from 50 KHz to 100 kHz
- Parity bit is even (optional)

#### Data Transmission Sequence:

1. Data from the encoder is sent with a MAX 491 transceiver in transmit mode. It is recommended to use any RS-422/485 compatible receiver and provide a termination resistor based on the RS-422/485 specification for your specific voltage and DATA line length.
2. The CLOCK signals are RS-422/485 compatible, differential TTL, with 180 Ohm termination resistors internal to the encoder. A series of pulses from the controller, on the CLOCK lines, advances the data.
3. On the first HIGH-to-LOW CLOCK transition, the encoder latches its data at the current position and prepares to transmit. The DATA signal during this transition is a START bit, which is always HIGH.
4. The encoder shifts data to the data line on each LOW-to-HIGH CLOCK transition, beginning with the MSB and ending with a "LO" bit (reference timing diagram). The controller reads data on the HIGH-to-LOW CLOCK transitions.
5. Additional CLOCK cycles following the "LO" bit will begin re-sending data, beginning with the MSB (reference timing diagram).
6. Parity is even. The sum of all logic "HI" data bits and the parity bit is even.
7. After the last CLOCK HIGH-to-LOW transition, a minimum of 65 microseconds must pass before the beginning of the next CLOCK series.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES APPLY AFTER FINISH TOLERANCES ON .XX ±.01      63 ✓ .XXX ±.005 ANGLES ± 0° 30' REMOVE BURRS AND BREAK ALL SHARP EDGES .010 MAX ALL DIA. TO BE © WITHIN .010	DRAWN      KRB APPR <i>[Signature]</i>	DATE 11/08/07 7-23-08	<b>BEI INDUSTRIAL ENCODER DIVISION</b> <b>BEI TECHNOLOGIES, INC.</b> 7230 Hollister Avenue   Goleta, CA 93117-2891   Tel: (805) 968-0782   Fax: (805) 968-3154			
	THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION OF BEI TECHNOLOGIES, INC. ANY REPRODUCTION, USE OR DISCLOSURE OF THIS DOCUMENT WITHOUT WRITTEN CONSENT OF BEI TECHNOLOGIES, INC. IS EXPRESSLY PROHIBITED.			TITLE      SPECIFICATION ADDENDUM SERIAL SYNCHRONOUS INTERFACE L18, 13 BIT (SSI)		
		SIZE      A FSCM NO.      1RB90 DWG NO.      924-02087-004 SCALE: NONE      924-02087-004-A.DWG	REV      A SHEET: 1/2			

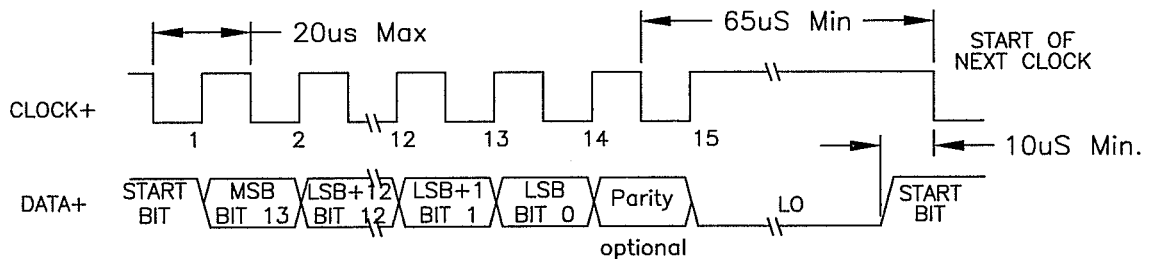
## Interfacing Long Data Lines:

Cable impedance creates a transmission delay, shifting the phase relationship between the clock pulse and the data. If this phase shift exceeds 180°, then the wrong bit position will be sampled by the receiver. The maximum allowable clock frequency, therefore, is a function of the cable length. EXAMPLE: for 24 AWG, stranded, 3 pair cable the group delay is 1.36nS/ft. The table below shows the maximum transmission rate allowable as a function of cable length to ensure a phase shift of less than 90°.

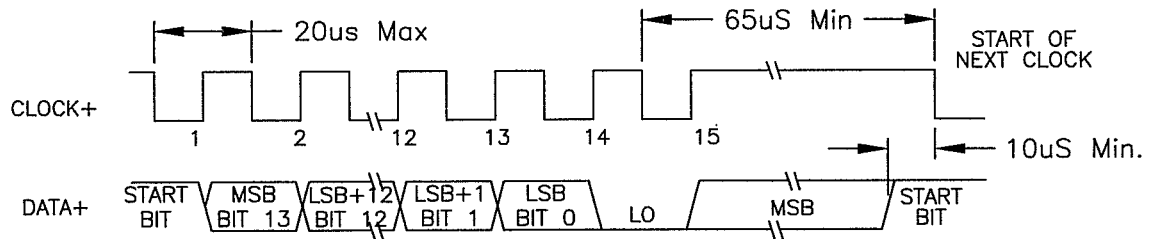
CLOCK: Maximum (KHz) = 92,000/Cable Length (ft)

Cable Length (feet)	1000	2000
Max. Frequency (KHz)	100	50

## SSI Compatible Output with Parity Option Timing Diagram:



13 BIT SSI with Parity Timing Diagram



13 BIT SSI without Parity Timing Diagram

## Output Wiring Diagram:

K8 CONN.	WIRE COLOR	FUNCTION
1	WHITE	DATA +
3	GREEN	DATA -
4	YELLOW	CLOCK +
5	GRAY	CLOCK -
6	PINK	DIR. CONTROL
* 8	RED	ENABLE
2	BROWN	+V (Supply Voltage)
7	BLUE	0V (Circuit Common)
	BARE	SHIELD DRAIN

\* = Optional

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